Chalcogenide Memory, Logic and Processing Devices

Prof C David Wright
Department of Engineering
University of Exeter
(david.wright@exeter.ac.uk)
Acknowledgements

University of Exeter – Yat-Yin Au, Jorge Vazquez, Mustafa Aziz, Krisztian Kohary, Rob Hicken, Yanwei Lui, Peter Ashwin

University of Oxford – Harish Bhaskaran, Peiman Hosseini

Chalcogenide (phase-change) memories

Sub-set of chalcogenide alloys known as *phase-change materials*

For typical phase-change alloys the *resistivity (and reflectivity) very different* between *crystalline* and *amorphous* states

We can *switch* (electrically and optically) between these states *quickly* and *reversibly*
Phase-change resistive memories

Information stored in **resistive state**

**Two states** for binary memory and logic

**Multiple states** for multi-level memory and processing

Resistive memories attractive:
- simple 2-terminal structure
- simple write/erase/read processes
- ideal for dense crossbar arrays
- 3D stackable

![Diagram of resistive switching layer, word line, and bit line]
Problem (& opportunity): The **access-time gap** between memory & storage

Towards a universal memory??

---

**Contexts – storage hierarchy**

<table>
<thead>
<tr>
<th>Access time (in ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU operations (1ns)</td>
</tr>
<tr>
<td>Get data from L2 cache (&lt;5ns)</td>
</tr>
<tr>
<td>Get data from DRAM/SCM (60ns)</td>
</tr>
<tr>
<td>Read a FLASH device (20 us)</td>
</tr>
<tr>
<td>Write to FLASH, random (1ms)</td>
</tr>
<tr>
<td>Read or write to DISK (5ms)</td>
</tr>
<tr>
<td>Get data from TAPE (40s)</td>
</tr>
</tbody>
</table>

**Near-future**

Near future technologies:

- **CPU**
- **RAM**
- **SCM**
- **DISK**
- **TAPE**

**Decreasing cost**

ON-chip memory

OFF-chip memory

ON-line storage

OFF-line storage
**Binary storage** - switch a small volume (the switching zone) of chalcogenide material from *completely amorphous* (RESET state) to *completely crystalline* (SET state) with a single electrical pulse.

Electrical switching from the amorphous state shows characteristic *threshold voltage*. 
SET (crystallisation) in PCM devices

Simulation of SET (crystallisation)
1.0 V, 100 ns set pulse

Brown – crystalline
Blue – initially amorphous

New crystal grains shown in various colours – each colour corresponds to different grain orientation

Extract electrical characteristics from simulation
Here show I-V curves for SET process

See C D Wright et al., APL 100, 253105 (2012)
Phase-change memories (cross-bar cells)

Vertical cross-bar cells

50 – 300 nm cells

See poster by Yat-Yin Au et al.
Phase-change memories (lateral cells)

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si3N4</td>
<td>10 nm</td>
</tr>
<tr>
<td>GST</td>
<td>30 nm</td>
</tr>
<tr>
<td>SiO2</td>
<td>100 nm</td>
</tr>
<tr>
<td>Si (100)</td>
<td></td>
</tr>
</tbody>
</table>

Lateral cells

Dielectric capping layer

Resistance vs number switching cycles
PCM – size scalability

3 nm diameter CNT electrodes
switching currents in µA range
switching energy in fJ range (100 fJ demonstrated)

see Xiong et al., Science 332, 569, 2011
PCM – speed scalability

Sub-ns switching also demonstrated in devices

See Loke .. Elliott et al., Science 336, 1566, 2012
Phase-change materials: new functionality?

Already established applications

- Optical storage (DVD-RAM, Blu-ray .....)
- Electrical phase-change memories (PCM)

Remaining issues to address: drift, power, speed, endurance, temperature stability

Possible future applications

- Phase-change logic
- Phase-change processors (arithmetic, neuromorphic)
- Mixed-mode (optical-electrical) devices
- Optical modulators/couplers/routers
- Integrated photonic memories and processors
- Phase-change displays
Phase-change logic

We can use **progressive crystallisation (accumulation)** to provide **logic functionality**

With a 2-terminal device can implement Boolean logic on serial data

**Example:** 4 input AND

Sample configuration

C-AFM tip as top electrode

Data sequence (purple)
Device switches after 4 pulses (green)
Equivalent to 4-input AND operation

Example:
2 input AND and OR operations

Advantages of this approach:
Non-volatile logic
Works with high number inputs (512)

Disadvantages:
Serial data – slow
Separate read out cycle

Alternatives:
Are being investigated to overcome these disadvantages

Multi-terminal phase-change logic

One alternative is to use multi-terminal devices - multiple/simultaneous inputs

AND/OR ‘GATE’

<table>
<thead>
<tr>
<th>IN1 (T1-T2)</th>
<th>Pulse type</th>
<th>logic level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crystallising</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Crystallising</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Amorphizing</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Amorphizing</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>IN2 (T1-T3)</th>
<th>Pulse type</th>
<th>logic level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crystallising</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Amorphizing</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Crystallising</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Amorphizing</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>OUT (T3-T2)</th>
<th>Resistance</th>
<th>Logic Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>High</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>High</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

NOT ‘GATE’

See S R Ovshinsky, Proceedings EPCOS 2010
Phase-change logic

Another alternative is to use **progressive amorphisation** (cf. progressive crystallisation)

Delivers much **faster logic** (but higher power consumption)

Example: **2 input NAND**

---

see Loke ... Elliott et al., PNAS 111, 13272, 2014
Progressive crystallisation (accumulation) can also be used to implement a **neuronal mimic**

Conventional silicon neuron circuits use ~ 10 to 20 CMOS gates

Phase-change neuron potentially much simpler-

*Self-resetting* phase-change neuron (SPICE simulation)

See C D Wright et al., Adv Func Mater 23, 2248 (2013)
Phase-change neuromorphics

The **multi-state regime** can be used to make phase-change **synaptic mimics**

New approach to computing using **bio-inspired (neuromorphic) processors**

Phase-change arithmetic processors

Using progressive crystallisation we can make a phase-change accumulator

With an accumulator we can perform all arithmetic operations

Accumulation (progressive crystallisation) with constant amplitude pulses

Here pulse amplitude and duration designed to make cell crystallise completely only after receipt of 10 pulses

C D Wright et al., Adv Funct Mater 23, 2248 (2013)
Addition with a base-10 accumulator

Example: $2_{10} + 5_{10} = 7_{10}$

(i) input pulses equal in number to 1st addend (2 in this case) : $\rightarrow$ cell left in state-2

(ii) input pulses equal in number to 2nd addend (5 in this case) : $\rightarrow$ cell left in state-7

Single phase-change cell simultaneously carries out addition and stores the result

To access the stored result:

(iii) Apply further (identical) pulses until the decision level is crossed ( $\rightarrow$ state-10)

The number of pulses required (3 in this case) and the base (10) yields the result

Specifically the complement of the number of pulses is the answer (7)

C D Wright et al., Adv Funct Mater 23, 2248 (2013)
Experimental accumulators

Top electrode diameter ~100 nm

Experimental I-V curve

C D Wright et al., Adv Funct Mater 23, 2248 (2013)
Accumulators in various bases

All pulses 100 ns duration (FWHM)
Different pulse amplitudes yield different base accumulators

Base-10 accumulator
Base-6, base-4 and base-2 accumulators

*C D Wright et al., Adv Funct Mater 23, 2248 (2013)*
Two-cell subtraction in base-6

Demonstration of the base-6 subtraction ($3_6 - 1_6$)

**METHOD**

*Three pulses* are input to Cell A

*One pulse* is input to Cell B.

Further pulses are applied to Cell A until it ‘switches’ (3 needed)

An identical number of pulses applied to Cell B - which will then be in state shown by green arrow.

Further pulses are applied until Cell B ‘switches’ - *two* are needed, which is our *answer*.

*C D Wright et al., Adv Func Mater 23, 2248 (2013)*
Arithmetic in optical domain

Performed **base-10** and **base-16** integer arithmetic - using **femtosecond** pulses

Efficient and powerful **non von-Neumann computing**

Non-integer arithmetic easily accomplished using multiple cells

e.g. Eight cells could represent the fixed-point number 0 to 9999.9999

Floating point numbers could also be represented

_C D Wright et al., Adv Mater, 23, 3408 (2011)_
Summary

Chalcogenide phase-change memories are attractive because they offer
Simple 2-terminal structure
2-D scalability to single-nm dimensions
3D architecture via simple cross-bar structure
Fast (sub ns) switching
Low energy (sub-pJ) switching
Good endurance (10⁶ to 10⁸)
Good retention (10 years at 80C)

Chalcogenides also offer attractive additional functionality including
Arithmetic and logic processing
Neuromorphic processing
Mixed-mode (optical-electrical) operation
All-photonic (phase-change) memories and computing
Solid state (phase-change) displays